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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,132	07/22/2003	Joseph M. Jeddeloh	501304.01	8276

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EXAMINER	
NGUYEN, MIKE	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 06/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,132	JEDDELOH, JOSEPH M.	
	Examiner	Art Unit	
	Mike Nguyen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) *3,10,19 and 30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-9,11-18,20-29 and 31-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
PRIMARY EXAMINER
GROUP 2100

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/28/05 & 4/21/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Notices & Remarks

1. Claims 1, 2, 4-9, 11-18, 20-29, and 31-34 are pending for the examination.

Election/Restrictions

2. Applicant's election without traverse of 1, 2, 4-9, 11-18, 20-29, and 31-34 in the reply filed on 02/01/2005 is acknowledged.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1, 2, 5, 8, 9, 13-15, 17, 18, 21, 24-26, 28, 29 and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by Talagala et al. (U.S. Pat. No. 6,845,409 B1).

As to claim 1, Talagala teaches a memory module (figs 1-3), comprising:

a plurality of memory devices (col. 8 lines 17-20); and

a memory hub (switch 14 of figs 1-3), comprising:

a link interface for receiving memory requests for access to at least one of the memory devices (host I/O port 18 of fig. 3);

a memory device interface coupled to the memory devices, the memory device interface coupling memory requests to the memory devices for access to at least one of the memory devices (multiple device I/O ports 20 of fig. 3);

a switch for selectively coupling the link interface and the memory device interface (switching elements 47 of fig. 3); and

a direct memory access (DMA) engine coupled through the switch to the memory interface device interface, the DMA engine generating memory requests for access to at least one of the memory devices to perform DMA operations (col. 9 lines 3-25).

As to claims 2, 9, 14 and 26, Talagala teaches an embedded system having the link interface, the memory device interface, the switch and the DMA engine residing in a single device (switch 14 of fig. 3).

As to claims 5, 21 and 32, Talagala teaches the plurality of memory devices is a bank of memory devices simultaneously accessed during a memory operation (col. 12 lines 28-43).

As to claim 8, Talagala teaches a memory hub for a memory module (switch 14 of figs 1-3) having a plurality of memory device (col. 8 lines 17-20), comprising:

a link interface for receiving memory requests for access to at least one of the memory devices (host I/O port 18 of fig. 3);

a memory device interface coupled to the memory devices, the memory device interface coupling memory requests to the memory devices for access to at least one of the memory devices (multiple device I/O ports 20 of fig. 3);

a switch for selectively coupling the link interface and the memory device interface (switching elements 47 of fig. 3); and

a direct memory access (DMA) engine coupled through the switch to the memory interface device interface, the DMA engine generating memory requests for access to at least one of the memory devices to perform DMA operations (col. 9 lines 3-25).

As to claim 13, Talagala teaches a memory system (figs 1-3), comprising:

a memory bus on which memory requests are provided (bus 22); and

at least one memory module coupled to the memory bus, the memory module having a plurality of memory device and a memory hub (switch 14), the memory hub comprising:

a link interface coupled to receive memory requests for access to at least one of the memory devices of the memory module on which the link interface is located (host I/O port 18 of fig. 3);

a memory device interface coupled to the memory devices, the memory device interface coupling memory requests to the memory devices for access to at least one of the memory devices (multiple device I/O ports 20 of fig. 3);

a switch for selectively coupling the link interface and the memory device interface (switching elements 47 of fig. 3); and

a direct memory access (DMA) engine coupled through the switch to the memory interface device interface, the DMA engine generating memory requests for access to at least one of the memory devices to perform DMA operations (col. 9 lines 3-25).

As to claims 15 and 25, Talagala teaches a high-speed memory bus (col. 7 lines 60-62).

As to claims 17 and 28, Talagala teaches the memory system of claim 13 wherein a plurality of memory modules are included in the memory system and a first memory module of the plurality of memory modules is couples to the memory bus and the remaining memory modules of the plurality are coupled in series with the first memory module (switches 14A and 14B of fig. 2).

As to claims 18 and 29, Talagala teaches the memory system of claim 13 wherein a plurality of memory modules are included in memory system and each of the plurality of memory modules are coupled directly to the memory bus through a respective link interface (fig. 2).

As to claim 24, Talagala teaches a computer system (figs 1-3), comprising:

a central processing unit ("CPU") (CPU 32 of fig. 2);

a system controller (controller 16 of figs 1 and 2) coupled to the CPU, the system controller having an input port and an output port (inherent);

an input device coupled to the CPU through the system controller (col. 8 lines 3-16);

an output device coupled to the CPU through the system controller (col. 8 lines 3-16);

a storage device coupled to the CPU through the system controller (col. 8 lines 3-16);

at least one memory module (figs 1-3), the memory module comprising:

a plurality of memory devices (col. 8 lines 17-20); and

a memory hub (switch 14 of figs 1-3), comprising:

a link interface coupled to receive memory requests for access to at least one of the memory devices of the memory module on which the link interface is located (host I/O port 18 of fig. 3);

a memory device interface coupled to the memory devices, the memory device interface coupling memory requests to the memory devices for access to at least one of the memory devices (multiple device I/O ports 20 of fig. 3);

a switch for selectively coupling the link interface and the memory device interface (switching elements 47 of fig. 3); and

a direct memory access (DMA) engine coupled through the switch to the memory interface device interface, the DMA engine generating memory requests for access to at least one of the memory devices to perform DMA operations (col. 9 lines 3-25); and

a communications link coupled between the system controller and at least one of the plurality of memory modules for coupling memory requests and data between the system controller and the memory modules (bus 22 of fig. 2).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4, 6, 7, 11, 12, 20, 22, 23, 31, 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Talagala in view of Jensen et al. (U.S. Pub. No. 2003/0149809 A1).

As to claims 4, 6, 7, 11, 12, 20, 22, 23, 31, 33 and 34, Talagala fails to explicitly teach a cross-bar switch, synchronous dynamic random access memory devices, an address registers, a target address location, a count register, and a next register. Jensen; however, teaches a cross-bar switch (paragraph [0040]), synchronous dynamic random access memory devices (paragraph [0036]), and DMA registers (elements 302-310 of fig. 3 and paragraph [0071]). It would have been obvious to a person of ordinary skill in the art to modify Talagala by the teaching of Jensen to include cross-bar switch, SDRAM and five register model in order to provide simultaneously accessing to the plurality memory devices, outputting burst data at a high data rate, and executing memory operation in the memory system without processor intervention, as expressly taught by Jensen at [0040] and [0036].

7. Claims 16 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Talagala in view of Fredriksson et al. (U.S. Pub. No. 2004/0236885 A1).

As to claims 16 and 27, Talagala fails to explicitly teach a high-speed optical memory bus and an optical memory bus interface circuit for translating optical signals and electrical signals. Fredriksson; however, teaches a high-speed optical memory bus and an optical memory

bus interface circuit for translating optical signals and electrical signals (paragraph [0044]). It would have been obvious to a person of ordinary skill in the art to modify Talagala by teaching of Fredriksson to include the high-speed memory bus and the optical memory bus interface circuit in order to provide possible for transmission with a great bandwidth, as expressly taught by Fredriksson at [009].

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Nguyen whose telephone number is 571 272-4153. The examiner can normally be reached on 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin can be reached on 571 272-4146. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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05/26/2005